Amendments to the Specification:

Please replace the paragraph on page 2 beginning on line 11 with the following amended paragraph.

In the present invention, the nitride storage element under the word gate is very small and well defined so that the hole injection for program is applicable over the whole nitride storage region. Erase is achieved by FN (Fowler-Norheim) electron injection, and once the nitride region is limited and optimized, then the voltage required for hole injection can be almost halved. By introducing a trap free oxide region between the two nitride storage sites, the threshold instability from program and erase cycles due to the miss match of hole and electron mean free paths is solved assuring high endurance. The voltage reduction in FN injection is achieved by reducing nitride thickness down to few atomic layers. Thus a low voltage and high density operation is achieved for the MONOS NAND structure of the present invention.

Please replace the paragraph on page 6 beginning on line 9 with the following amended paragraph.

This invention will be described with reference to the accompanying drawings, wherein:

FIG. 1A shows a diagram of a portion of a floating gate NAND memory array of prior art,

FIG. 1B and 1C shows a diagram of a portion of a floating gate NAND memory array where the floating gate area is constructed using an ONO region under the control gate[.],

FIG. 2 shows a schematic diagram of a twin MONOS NAND memory array of the present invention,

FIG. 3A and 3B show diagrams of the memory array structure of the present invention[.],

FIG. 4A shows a diagram for an erase operation of a memory cell of the present invention, where device 31 and 32 are both charged with electrons by FN tunnel injection,

FIG. 4B shows a diagram for a program operation of a memory cell of the present invention, where a device is programmed by hot hole injection generated by band to band tunneling,

FIG. 5A shows a schematic diagram for a program operation of a selected cell in the memory array of the present invention,

FIG. 5B shows a schematic diagram for an erase operation of a block of cells in the memory array of the present invention,

FIG. 6A shows a diagram of three device components in a single memory cell of the present invention,

FIG. 6B shows a table of possible threshold conditions in the three devices in a single memory cell including the net threshold of the combined memory cell[.],

FIG. 6C shows the threshold behavior of a memory cell for different memory storage states provided in FIG.6B[.],

FIG. 7 shows a schematic diagram for a read operation of a selected cell in the memory array of the present invention, and

FIG. 8A through 8I show process steps to produce the twin MONOS memory cell of the present invention.

Please replace the paragraph on page 13 beginning on line 12 with the following amended paragraph.

FIG. 8A, through 8F show a fabrication method for an N channel Twin MONOS memory array. In FIG. 8A a P-type silicon substrate 90 is doped with the surface concentration in the range of approximately about 5E17 to 1.5E18 atoms per cm^3. Shallow trench isolation (not shown) is formed in areas between columns of memory cells. Then a gate oxide 91 in the range of approximately about 2nm to 5nm is grown. A polysilicon layer 92 in the range of approximately between of 150nm to 250nm is CVD (chemical vacuum deposited) followed by a nitride deposition 93 in the range of approximately about 100nm to150nm. The photo resist [94] <u>89</u> is patterned to define areas for an N+ deposition using conventional photolithography.

Please replace the paragraph on page 13 beginning on line 21 with the following amended paragraph.

Referring to FIG. 8B, the nitride and the polysilicon are etched using the photo resist [94] <u>89</u> as a mask. Then As (arsenic) is implanted at a concentration of approximately between 3E12 and 3E13 atoms per cm^3 at an energy level of approximately between 15keV and 20keV to create a lightly doped region 94. After the lightly doped regions are implanted, an oxide layer [of] in the range of approximately about 30nm to 60nm is deposited by CVD and etched vertically leaving sidewall spacers

95 having a thickness of approximately between 25nm to 55nm, which suppresses the out diffusion of N+ under the nitride storage region. A heavily doped N+ region 96 is implanted with As to a concentration of approximately about 1.5E15 atom per cm^3 at an energy level between approximately 15keV and 25keV.

Please replace the paragraph on page 14 beginning on line 8 with the following amended paragraph.

In FIG. 8C a CVD oxide 98 in thickness in the range of approximately between 250nm and 400nm is deposited, and then the oxide 98 is chemically mechanically polished (CMP) <u>to planarize the surface of the substrate</u>, stopping at nitride 93 <u>when the mask elements are detected</u>. The oxide isolation layer 98 is self-aligned to the diffusions 94 and 96.

Please replace the paragraph on page 14 beginning on line 12 with the following amended paragraph.

Referring to FIG. 8D, the nitride layer 93 is selectively removed, and the, polysilicon 92 is also carefully and selectively etched out by a chemical dry etch. The remaining oxide 91 of a thickness of approximately 3.0nm is etched out. Then a fresh gate oxide 100 having a thickness of approximately between 2.5nm and 5nm is thermally grown followed by nitride deposition [100] <u>101</u> to a thickness of approximately between 3nm and 9nm. A disposable sidewall spacer (DWS) 102 is <u>formed on the sidewalls of the nitride 101 by depositing a spacer material</u> [deposited] to a thickness of approximately between 25nm and 40nm using a material such as polysilicon, BPSG

(borophosphosilicate glass) or oxynitride, which can be selectively etched against the silicon oxide isolation layer 98. After the spacer 102 is etched, exposed areas of the nitride layer 101 are etched out using the DSW as the mask.

Please replace the paragraph on page 14 beginning on line 22 with the following amended paragraph.

Referring to FIG 8E, after the DSW 102 is selectively removed, the ~~remained~~ <u>remaining</u> nitride layer 101 and bottom silicon 100 are oxidized 103 by ISSG (InSitu Steam Generation) tool and an additional thermal oxidation is used to grow approximately between 5nm and 6nm on the nitride 101. A thickness of approximately between 3nm and 4nm of the nitride 101 is converted to a thickness of approximately between 5nm and 6nm of oxide. The remaining nitride thickness after ISSG oxidation is a range approximately between few atomic layers and 6nm. The oxide is also grown on the exposed substrate silicon regions in between the L-shaped nitride pair to approximately between 8nm and 12nm.

Please replace the paragraph on page 16 beginning on line 18 with the following amended paragraph.

Referring to FIG. 8I, a barrier metal such as titanium nitride [and] <u>or</u> tungsten 111 is deposited to connect side wall polysilicon 108 and polysilicon 110 into a word gate and to connect to agate polysilicon in the peripheral area (not shown), followed by CMP (chemical mechanical polish) to remove unnecessary tungsten. The process sequence can be shared with a contact stud process.